## IN THE CLAIMS

Please amend the claims as set forth below:

1-20. (Cancelled)

21. (Previously Presented) A high-availability cellular computer system capable of automatically updating firmware in cells of the system, the system comprising:

a high speed interconnect;

a first cell and a second cell, each cell comprising at least one processor coupled to

at least one random-access memory subsystem,

at least one nonvolatile memory system, and

a high-speed interconnect interface;

wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect; and

wherein the nonvolatile memory subsystem of the first cell has recorded therein corrupt firmware, and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware; and

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is corrupt and, upon recognizing that the firmware of the first cell is corrupt, for updating the nonvolatile memory system of the first cell with firmware copied from a cell having valid firmware; and

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid, and for transmitting the firmware in the nonvolatile memory system of the second cell to the first cell.

22. (Previously Presented) The system of claim 21 further comprising:

a manageability system interconnect;

wherein the first cell and the second cell further comprise a management processor;

wherein the management processor of the second cell contains machine readable code to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect, to enable the high speed interconnect; and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect.

23. (Currently Amended) The system of claim 21 further comprising:

a manageability system interconnect;

wherein the first cell and the second cell further comprise a management processor;

wherein the management processor of the second cell contains machine readable code to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect, ~~to enable the high speed interconnect;~~ and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the manageability system interconnect.

24. (New) A high-availability cellular computer system capable of automatically updating firmware in cells of the system, the system comprising:

a high speed interconnect;

a first cell and a second cell, each cell comprising at hardware level:

at least one processor of the cell coupled to at least one random-access memory subsystem of the cell,

at least one nonvolatile memory system coupled to the at least one processor of the cell,

a high-speed interconnect interface coupling the at least one processor of the cell to the high speed interconnect,

wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect; and

wherein the nonvolatile memory subsystem of the first cell has recorded therein corrupt firmware, and the nonvolatile memory subsystem of the second cell has recorded therein valid firmware; and

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is corrupt and, upon recognizing that the firmware of the first cell is corrupt, for updating the nonvolatile memory system of the first cell with firmware copied from a cell having valid firmware; and

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid, and for transmitting the firmware in the nonvolatile memory system of the second cell to the first cell.

25. (New) The system of claim 24 further comprising:

a manageability system interconnect;

wherein the first cell and the second cell further comprise a management processor;

wherein the management processor of the second cell contains machine readable code to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect, to enable the high speed interconnect; and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect.

26. (New) The system of claim 24 further comprising:

a manageability system interconnect;

wherein the first cell and the second cell further comprise a management processor;

wherein the management processor of the second cell contains machine readable code to receive an update message via the manageability

system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect, and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the manageability system interconnect.